PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Elisa J. Collins; Lee Houck; Jonathan Adersh; Faith Kinoglu	Confirmation No.	9002
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Docket No.:	57205US002 (1004-030US01)		
Title:	OPERATOR ADVISORY SYSTEM (OASys)		

CERTIFICATE UNDER 37 CFR 1.8: I hereby certify that this correspondence is being deposited with the United States Post Service, as First Class Mail, in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450 on October 27, 2005.

By: Patricia Cygan
Name: Patricia Cygan

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants respectfully request a Pre-Appeal Brief Request for Review, based upon the Examiner's failure to establish a prima facie case of anticipation under 35 U.S.C. §102. As outlined in greater detail below, the applied reference fails to disclose one or more claimed elements. For this reason, the anticipation rejections under 35 U.S.C. §102 are clearly improper and must be reversed.

Claims 1-35 stand rejected under 35 U.S.C. §102(b) as being anticipated by Parson et al. (US 6,053,947). This rejection is improper insofar as Parson fails to disclose simulating a manufacturing process as required by each of the independent claims.

Before addressing the details of the claim rejections, Applicant provides the following brief summary of Parson. In general, the disclosure of Parson is related to techniques for

modeling a circuit using a computer-based simulator. In particular, Parson describes simulating a single circuit by, upon a change in a signal, performing subcircuit simulations that use the signal according to a hierarchy.[1] A circuit is clearly not a manufacturing process. As such, Parson fails to teach or suggest simulating a manufacturing process as recited by each of Applicants' independent claims. Parson is not even related to simulation of a manufacturing process. In this most basic fashion, all of Applicants' claims are distinct over the disclosure of Parson.

Claims 1-35

Claim 1 recites a system comprising a set of objects encapsulating respective computational models that simulate a manufacturing process, wherein each of the models receives one or more inputs values and computes one or more predicted output values based on the simulation, and a software program executing within a computer operating environment and having an embedded control module to invoke the computational models in parallel to produce the predicted output values computed by the encapsulated computational models.

In general, Parson fails to teach any mechanism for simulating a manufacturing process, let alone the use of objects to encapsulate separate models and invocation of those models in parallel. In contrast, Parson describes techniques for simulating the operation of an electrical circuit.[2] For example, Parson defines a circuit as a combination of electrical components that cooperate to perform a particular function.[3] A circuit is not a manufacturing process, and claim 1 is novel over the disclosure of Parson in this respect.

Moreover, Parson also fails to describe a system where computational models are each encapsulated in respective objects, i.e., where a single, respective object encapsulate each model in the models entirety. Instead, Parson describes modeling a circuit using software objects. Parson discloses producing a single model of a circuit; the model including interconnected objects in a hierarchical relationship.[4] This is fundamentally different than Applicants' disclosed and claimed invention.

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[1] See, *e.g.*, Parson, Abstract.
[2] See, *e.g.*, Parson, Abstract.
[3] Parson, column 1, lines 24-26.
[4] See, *e.g.*, Parson, column 4, line 65.

This distinction may be best illustrated by another clause in Applicants' claim 1, which requires invoking the computational models in parallel. Similarly, claim 25 also requires invoking the set of objects from the control module to execute the computational models in parallel.

In contrast, Parson describes a hierarchy of a circuit model containing subcircuit models.[5] As such, Parson requires subcircuit objects to be executed according to the hierarchy, presumably because the output of one object may be required as an input to execute another object. The Examiner referred to nesting of scheduler models, and asserted that bundling their contents within the scheduler as illustrating that Parson discloses invoking the computational models in parallel. However, this interpretation is inconsistent with the disclosure of Parson. As stated in Parson, "[a] scheduler model is an infrastructure class representing the outer or root level of a design hierarchy."[6] In Parson, nesting of scheduler models is a means to combine scheduler models. Nesting is not execution of models in parallel, but rather a means to combine sub-models to create a single combined model that is different from models used to produce it.

Consequently, nested scheduler models must be combined with subcircuit models to produce a single simulated circuit model. In this manner, a scheduler model of Parson is not itself a computational model, but means to define a hierarchical arrangement between subcircuit models to produce a single simulation model.

Because claims 1-35 each require modeling a manufacturing process, Parson does not disclose the subject matter of any of claims 1-35. Therefore, the Examiner's rejection of claims 1-35 under 35 U.S.C. §102(b) in view of Parson is in error.

Response to Examiner Comments

In the Advisory Action dated October 17, 2005, the Examiner stated, "Similating (sic) /Modeling a Circuit (taught by Parson) is considered a manufacturing process (for example, see Applicants' definition in the first paragraph of the specification) and col. 1 lines 14-18 of the Parson reference." The Examiner's use of the term "manufacturing process" is inconsistent with

[5] Parson, column 4, lines 62-63.
[6] Parson, column 9, lines 36-37.

the plain language of Applicants' claims, the context provided by Applicants' disclosure and even the teaching of Parson itself.

Claims terms are generally given their ordinary meaning.[7] In *Phillips v. AWH Corporation*, the Court addressed the proper interpretation of the "ordinary meaning" of a claim. Specifically, in *Phillips*, the Court made clear that the "ordinary meaning" of a term is the meaning to one of ordinary skill in the art not only in the context of the particular claim but in the context of the entire patent, including the specification.[8] The Court reiterated that the specification is the "primary basis for construing the claims."[9] According to the Court, when properly viewed, the "ordinary meaning" of a claim term is its meaning to the ordinary artisan after reading the entire patent. Heavy reliance on dictionaries or other extrinsic evidence risks transforming the meaning of a claim term out of its particular context, which is the specification.[10]

The Examiner's conclusion that Parson discloses subject matter within the scope of claims 1-35 is clearly improper. The Examiner cited the first paragraph of Applicants' specification as support for the premise that a circuit may be a "manufacturing process". Yet, Applicants' specification does not suggest that a circuit can be a manufacturing process here or anywhere else. The Examiner's construction of the term "manufacturing process" in Applicants' claims is erroneous. Accordingly, the rejection of claims 1-35 is in error for failing to teach numerous elements of Applicants' claims.

CONCLUSION

The Examiner's rejection of claims 1-35 under 35 U.S.C. §102(b) as being anticipated by Parson is in error. Applicant requests a review and a panel decision that promptly resolves the issues in Applicants' favor and eliminates the need for an Appellate Brief. For at least the reasons set forth above, all rejections must be reversed.

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[7] *Vitronics*, 90 F.3d 1582.
[8] Phillips v. AWH Corporation, No. 03-1269 (Fed. Cir. July 12, 2005) (en banc).
[9] *Phillips*, at 14 (citing Standard Oil Co. v. Am. Cyanamid Co., 774 F.2d 448, 452 (Fed. Cir. 1985).
[10] *Id.*

By setting forth the clear grounds of error, Applicant does not assert that these are the only errors that the Examiner has made, nor does Applicant waive any arguments that may be asserted in an Appeal Brief.

Please charge any additional fees or credit any overpayment to deposit account number 50-1778.

Date:
October 27, 2005

By:

SHUMAKER & SIEFFERT, P.A.
8425 Seasons Parkway, Suite 105
St. Paul, Minnesota 55125
Telephone: 651.735.1100
Facsimile: 651.735.1102

Name: Kent J. Sieffert
Reg. No.: 41,312